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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,112	06/26/2003	Shahid Butt	FIS920030087	1111

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EXAMINER	
LEE, EUGENE	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 08/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,112	BUTT ET AL.	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22 and 30-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22 and 30-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2003* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, a transistor ... comprising functional gate conductors (i.e. claim 1) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

It appears (i.e. FIG. 1A) there are multiple transistors each having a single functional gate conductor, however, the figures do not show a single transistor which has multiple functional gate conductors.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1 thru 22, and 30 thru 33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 1, and 12, it is unclear how the applicant defines a transistor. From FIG. 1A, it appears that there are **multiple** transistors (each having a source and drain) that use a functional gate conductor, however, it is not a single transistor (i.e. "transistor in a substrate") that comprises functional gate conductors. Appropriate clarification and/or correction are required.

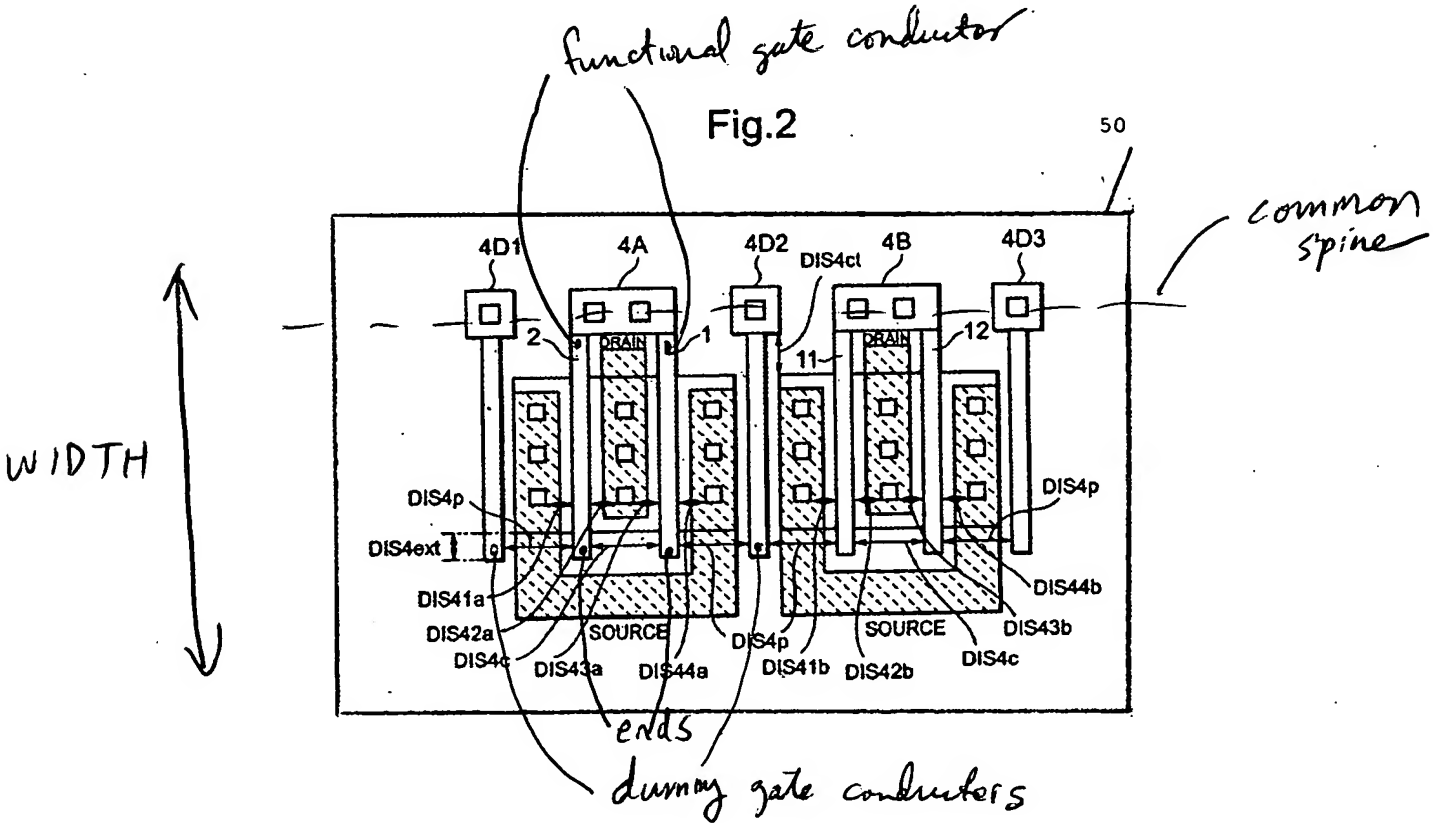
Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Insofar as definite, claims 1, 4 thru 12, and 15 thru 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki 6,833,595 B1 in view of Uehara et al. 5,946,563. Iwaskai discloses (see, for example, Fig. 2) a semiconductor device (electronic device) comprising a semiconductor substrate, transistor 4A, gates (functional gate conductors) 1, 2, common spine, dummy gates (dummy gate conductors) 4D1, 4D2, and element isolation region (insulating layer) 50. The gates extend in a widthwise direction from a common spine, the common spine

extending in a direction perpendicular to said widthwise direction. The gates are positioned substantially parallel to each other in said widthwise direction and periodically spaced apart a fixed distance in said direction substantially perpendicular to said widthwise direction. The dummy gates are positioned substantially parallel to each other in a widthwise direction and periodically spaced apart a fixed distance in a direction substantially perpendicular to said widthwise direction. The dummy gates are not positioned between gates 1, 2 and adjacent to ends of said gates.



Iwaskai does not disclose said dummy gates positioned over a gate dielectric layer over a trench formed in said semiconductor substrate. However, Uehara discloses (see, for example, Fig. 6) a semiconductor device comprising a transistor, dummy electrodes (dummy gates) 50b, dummy insulating films (gate dielectric layer) 15b, trench, and isolation (insulating layer) 17. In the

abstract, Uehara discloses that with the dummy electrodes, any gate electrode can be formed in a line-and-space pattern, so that the finished sizes of the gate electrode become uniform in order to reduce gate length, and hence, a semiconductor device of higher integration which is operable at a higher speed and substantially free from variation in finished size resulting from the use of different gate patterns. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have said dummy gates positioned over a gate dielectric layer over a trench formed in said semiconductor substrate in order so with the dummy electrodes, any gate electrode can be formed in a line-and-space pattern, so that the finished sizes of the gate electrode become uniform in order to reduce gate length, and hence, a semiconductor device of higher integration which is operable at a higher speed and substantially free from variation in finished size resulting from the use of different gate patterns.

Regarding claims 4, and 15, see, for example, Fig. 2 wherein Iwasaki discloses the dummy gates 4D1, 4D2, and gates 1,2 having the same gate widths.

Regarding claims 5, 6, 16, and 17, see, for example, Fig. 2 wherein Iwasaki discloses dummy gate (additional dummy gate conductors) 4D3.

Regarding claims 7, 8, 18, and 19, Iwasaki in view of Uehara does not disclose the length of said functional gate conductors being a function of positive integer multiples of a minimum length of said gate conductors and of positive integer multiples of said fixed distance, and the length of said dummy gate conductors being a function of positive integer multiples of a minimum length of said gate conductors and of positive integer multiples of said fixed distance. However, it was well within the skills of an artisan in the art to optimize the performance of a semiconductor device by adjusting the length of said functional gate conductors and dummy gate

conductors in order to minimize proximity effect, and improve manufacture of a semiconductor device. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have the length of said functional gate conductors being a function of positive integer multiples of a minimum length of said gate conductors and of positive integer multiples of said fixed distance, and the length of said dummy gate conductors being a function of positive integer multiples of a minimum length of said gate conductors and of positive integer multiples of said fixed distance because it was well within the skills of an artisan to optimize the performance of a semiconductor device by adjusting the length of said functional gate conductors and dummy gate conductors in order to minimize proximity effect, and improve manufacture of a semiconductor device. See In re Aller, 105 USPQ 233.

Regarding claims 9, 10, 20, and 21, see, for example, Fig. 2 wherein Iwasaki discloses source/drains SOURCE /DRAIN.

Regarding claims 11, and 22, transistors have a gate dielectric in between the gate conductor and substrate in order to form a channel in the substrate.

6. Claims 2, 3, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki '595 B1 in view of Uehara et al. '563 as applied to claims 1, 4-12, and 15-22 above, and further in view of Fukuda 6,660,462 B1. Iwasaki in view of Uehara does not disclose gate conductors of at least two different gate widths, and dummy gate conductors of at least two different widths. However, Fukuda discloses (see, for example, FIG. 4A) transistor gate patterns (functional gate conductors) 18, and dummy gate patterns (dummy gate conductors) 19 of varying widths. In column 7, lines 6-12, Fukuda discloses the patterns do not cause variation in

line width by the proximity effect. Therefore, it would have been obvious to one of ordinary skill in the art to have gate conductors of at least two different gate widths, and dummy gate conductors of at least two different widths in order to not cause variation in line width by the proximity effect.

7. Claims 30 thru 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki '595 B1 in view of Uehara et al. '563 as applied to claims 1, 4-12, and 15-22 above, and further in view of Kang 6,872,990 B1. Iwasaki in view of Uehara does not disclose two adjacent dummy gates being integrally connected in a "U" shaped pattern wherein said two adjacent dummy gates are of different gate widths. However, Kang discloses (see, for example, FIG. 12) dummy gates DG1 having a U-shape wherein the widths are different. In column 5, lines 55-58, Kang discloses dummy gates minimize variances in the process deviations which may occur in the photo and etching processes for the production of the semiconductor device. Therefore, it would have been obvious to one of ordinary skill in the art to have disclose two adjacent dummy gates being integrally connected in a "U" shaped pattern wherein said two adjacent dummy gates are of different widths in order to minimize variances in the process deviations which may occur in the photo and etching processes for the production of the semiconductor device

Response to Arguments

8. Applicant's arguments with respect to claims 1-22, and 30-33 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eugene Lee
July 28, 2005